IN THE ABSTRACT:

Please amend the abstract as follows:

Disclosed is a method and system for ~~wafer/probe~~ testing ~~of~~ integrated circuit devices after manufacture. ~~The invention begins by testing~~, wherein an initial group of devices ~~(e.g., integrated circuit chips)~~ is tested to produce an initial failing group of devices that failed the testing. The devices in the initial failing group are identified by type of failure. Then, ~~the invention retests~~ the devices in the initial failing group are retested to identify a retested passing group of devices that passed the retesting. Next, ~~the invention analyzes~~ the devices in the retested passing group ~~which allows the invention~~ are analyzed to produce statistics regarding the likelihood that a failing device that failed the initial testing will pass the retesting according to the type of failure. Then, ~~the invention evaluates~~ these statistics are evaluated to determine which types of failures have retest passing rates above a predetermined threshold. From this, ~~the invention produces~~ a database is produced that includes ~~comprising~~ an optimized retest table listing the types of defects that are approved for retesting.